REMARKS

The Office Action mailed on April 16, 2002, has been received and reviewed. Claims 17-33, 50-72, and 74-101 are currently pending in the above-referenced application. Each of claims 17-33, 50-72, and 74-101 stands rejected.

Reconsideration of the above-referenced application is respectfully requested.

Drawings

The Drawings have been objected to under 37 C.F.R. § 1.83(a) for not showing every feature of the invention specified in the claims.

In particular, it was asserted that the drawings do not depict "laterally discrete, spaced apart regions", as recited in the currently pending claims of the above-referenced application. It is respectfully submitted that FIG. 4 already shows that spaced apart regions 14a and 14b are laterally discrete from one another. Nonetheless, it is proposed that the drawings be corrected to include a new FIG. 4A, which is submitted herewith under cover of a separate Letter to the Official Draftsperson. It is respectfully submitted that FIG. 4A adds no new matter, but merely serves to more clearly illustrate features of the invention. Specifically, FIG. 4A more clearly illustrates the "spaced apart regions [14a, 14b] of a first layer of conductive material around and between which an underlying insulative structure [4] is exposed" as being laterally discrete from one another. This is done in the same manner as in FIG. 7, but without the overlying features that are formed from layer 16 of conductive material.

Approval and entry of FIG. 4A are respectfully requested.

It is respectfully submitted that, even without approval and entry of FIG. 4A, that the drawings (particularly FIG. 4) of the above-referenced application depict all of the elements that are recited in the claims and, thus, comply with the requirements of 37 C.F.R. § 1.83(a).

35 U.S.C. § 112 Claim Rejections

Claims 17-33, 50-72, and 74-101 stand rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Applicant respectfully traverses this rejection, as hereinafter set forth.

The fabrication of spaced apart regions 14a and 14b is described, for example, at page 9, line 16, to page 10, line 7, of the originally filed specification. Subsequently, a layer 16 of conductive material is formed over spaced apart regions 14a and 14b. *See, e.g.,* page 10, line 15, to page 11, line 6. Next, layer 16 may be patterned without patterning the remaining portions of the underlying layer 14, from which spaced apart regions 14a and 14b are formed. *See* page 11, lines 11-13. The resulting structure is depicted in FIG. 7, which clearly depicts spaced apart regions 14a and 14b as being laterally discrete from one another.

Accordingly, it is respectfully submitted that the originally-filed specification provides sufficient support for the subject matter recited in the claims of the above-referenced application and requested that the 35 U.S.C. § 112, first paragraph, rejection of claims 17-33, 50-72, and 74-101 be withdrawn.

Rejections Under 35 U.S.C. § 103(a)

Fischer in View of Chen

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on

applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

Claims 17, 19-24, and 26-33 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 5,185,291 to Fischer et al. (hereinafter "Fischer") in view of U.S. Patent 5,712,206 to Chen (hereinafter "Chen").

Fischer teaches a fuse for use in a semiconductor device structure, as well as a process for fabricating the fuse. The fuse of Fischer, which is disposed over an insulative structure (dielectric 10, *see, e.g.,* FIGs. 1-4; col. 2, lines 29-36), includes a first conductive layer 11 and a second conductive layer 12. The first conductive layer 11 of the finished fuse may be formed from aluminum or tungsten (col. 2, lines 43-45) and includes two spaced apart end regions (FIG. 3). The second conductive layer 12 of the fuse is typically formed from the same material as the first layer 11, but may also be formed from polysilicon (col. 2, lines 59-63). In a finished fuse, such as that illustrated in FIG. 3 of Fischer, end portions of the second conductive layer 12 overlie the spaced apart regions of the first conductive layer 11, while the central portion 111 of the second conductive layer 12 is located in substantially the same plane as the first conductive layer 11 and between the spaced apart portions of the first conductive layer 11 (*see also,* col. 2, lines 56-58).

Fischer teaches that the fuse may be fabricated by forming a first layer of conductive material 11 over an insulative structure 10 (FIG. 1; col. 2, lines 45-48), patterning a "window" 111 in the first layer of conductive material to expose a portion of the underlying insulative structure (FIG. 1; col. 2, lines 36-38; col. 3, lines 34-55), forming a second layer 12 of conductive material over the first layer 11 and within the window 111 (FIG. 2; col. 2, lines 49-55), and patterning the "combined" first and second layers to form the fuse (FIG. 3; col. 2, lines 56-58). The first conductive layer is not patterned to form laterally discrete, spaced apart regions, rather a continuous surface with a window, until after the second layer has been deposited.

Chen teaches a method of forming a moisture barrier system for an integrated circuit on a substrate having a fuse window area. A field oxide region is formed over a substrate, a first insulating layer over the field oxide layer, a barrier layer over the first insulating layer, next, an interlevel dielectric layer is formed over the barrier layer, a second barrier layer is formed over the interlevel dielectric layer. Finally, a fuse, preferably composed of aluminum or titanium tungsten, a silicide (*e.g.,* tungsten silicide, platinum silicide, etc.,), polysilicon, or a polycide (*e.g.,* titanium polycide, tungsten polycide, molybdenum polycide, etc.) is formed over the second barrier layer. The fuse 62 is a single layer of uniform thickness and width. *See* FIGs. 1B, 2. The fuse is burnt open in the fuse window. Col. 4 line 53.

Independent claim 17 recites a method for fabricating a fuse. The method of claim 17 includes, among other things, patterning a layer of conductive material to define at least two laterally distinct, spaced apart regions, between and around which an underlying insulative structure is exposed. The method of claim 17 also includes disposing a layer of metal silicide over and between the two regions of conductive material.

One of Ordinary Skill in the Art Would Not Have Been Motivated to Make the Proposed Combination

It is respectfully submitted that one of ordinary skill in the art would not have been motivated to combine the teachings of Fischer and Chen in the manner that has been asserted in the outstanding Office Action.

Specifically, it is respectfully submitted that one of ordinary skill in the art would not have been motivated to substitute one of the metal silicides described in Chen for the formation of an aluminum, tungsten, or polysilicon layer in the fuse fabrication process described in Fischer, thereby using metal silicide in place of the aluminum, tungsten, or polysilicon of Fischer as the portion of a fuse that is to be ruptured.

While it is acknowledged that a fuse composed of a single metal silicide layer of uniform thickness and width is suggested in Chen, this fact in and of itself would not have motivated one of ordinary skill in the art to substitute tungsten silicide for materials such as aluminum or tungsten in a fuse comprising multiple layers of conductive material. By touting the usefulness of aluminum, tungsten and polysilicon as the second, programmable material layer of the fuse disclosed therein, Fischer clearly fails to provide any motivation to one of ordinary skill in the art to find a substitute for these materials.

It is, therefore, respectfully submitted that one of ordinary skill in the art would not have been motivated to modify the fuse fabrication method described in Fischer by forming a metal silicide layer, rather than the polysilicon layer described. Consequently, it appears that any motivation to combine the teachings of Fischer and Chen could only have been based on hindsight provided by the specification or claims of the above-referenced application.

The Proposed Combination Does Not Teach or Suggest Each and Every Claim Element

It is further submitted that the combination of Fischer and Chen fails to teach or suggest each and every element of independent claim 17.

In contrast to the subject matter recited in independent claim 17, neither Fischer nor Chen, taken alone or in combination, teaches a fuse fabrication method that includes patterning a layer of conductive material to form at least two laterally discrete, spaced apart regions with an underlying insulative structure exposed therethrough and formed therearound. Rather, the teachings of Fischer are limited to forming a *window* using local etching of a conductive layer, which could not result in laterally discrete, spaced apart regions of a first layer of conductive material around and between which an underlying insulative structure is exposed. According to Fischer, no laterally discrete, spaced apart regions of the first layer of conductive material are formed until after the second layer of conductive material has been formed and, thus, the underlying insulative structure is never exposed between these laterally discrete, spaced apart regions of the first layer of conductive material.

Chen neither teaches nor suggests patterning a layer of conductive material to fabricate a fuse.

As neither Fischer nor Chen teaches or suggests patterning a layer of conductive material to define two or more laterally discrete, spaced apart regions of conductive material with an insulative structure exposed therebetween, it would be impossible to combine these references to teach patterning a layer of conductive material in such a fashion.

No Reasonable Expectation of Success

Moreover, even assuming, *arguendo,* that one of ordinary skill in the art would have been motivated to combine the teachings of Fischer and Chen in the manner that has been asserted in the outstanding Office Action, it is respectfully submitted that one of ordinary skill in the art would not reasonably expect that Fischer and Chen could be successfully combined in such a way as to render obvious the subject matter recited in amended independent claim 17. Again assuming, for the purpose of argument, that the asserted combination of Fischer and Chen might result in the same structure as a structure that may be formed by the method recited in amended independent claim 17, the combination of Fischer and Chen could not result in a method in which a layer of conductive material is patterned "to define at least two laterally discrete, spaced apart regions of conductive material between and around which [an underlying] insulative structure is exposed . . ."

Further, since the Fisher method of fuse formation requires that both the first and second conductor layers are etched in one operation, (Col. 3, lines 59-65) there is no reasonable expectation of success etching a first conductive layer of aluminum or tungsten and a second layer of metal silicide in one operation.

For these reasons, it is respectfully submitted that, under 35 U.S.C. § 103(a), claim 17 is allowable over the combination of Fischer and Chen.

Claims 19 through 24, and 26 through 33 are each allowable, among other reasons, as depending either directly or indirectly from claim 17, which should be allowed.

In view of the foregoing, it is respectfully requested that the Office withdraw the rejections of claims 17, 19 through 24 and 26 through 33 under 35 U.S.C. § 103(a).

Fischer, Chen, and Further in View of Mitani

Claim 18 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Fischer and Chen as applied to claim 17 above, and further in view of Japanese Patent No. 59-154,038 to Mitani (hereinafter "Mitani").

The teachings of Fischer and Chen have been summarized above.

Mitani teaches a method for fabricating a fuse, which includes a central region formed of polycrystalline silicon. First the polycrystalline silicon is deposited on a field oxide film. Next, a layer of metal silicide is formed over the polycrystalline silicon, and the layers are etched in combination. Finally, the intermediate part of the metal silicide is etched, leaving only polycrystalline silicon as the central region of the finished fuse, the portion of the fuse that is to be ruptured.

Claim 18 is allowable, among other reasons, as depending from claim 17, which should be allowed.

It is also respectfully submitted that there are several additional reasons that the combination of Fischer, Chen, and Mitani does not render the subject matter recited in claim 18 obvious.

One of Ordinary Skill in the Art Would Not Have Been Motivated to Make the Proposed Combination

First, it is respectfully submitted that one of ordinary skill in the art would not have been motivated to combine the teachings of Mitani with those of Fischer or Chen in the manner that has been asserted in the outstanding office action. In particular, it is not understood how or why one of ordinary skill in the art would have been motivated to incorporate the teachings from a

reference (Mitani) which teaches a method for fabricating a fuse having polysilicon as the portion of the fuse that is to be ruptured and spaced apart regions of metal silicide into a reference (Fischer) that teaches a method for fabricating a fuse also having polysilicon as the portion of the fuse to be ruptured and spaced apart regions of aluminum or tungsten in a manner resulting in a fuse having metal silicide as the portion of the fuse that is to be ruptured and spaced apart regions of polysilicon. Chen discloses a fuse having a metal silicide as the portion of the fuse to be ruptured, however this fuse has no spaced apart regions of conductive material.

In any event, Mitani does not supply the motivation that is missing from both Fischer and Chen; patterning a first conductive layer to define at least two laterally discrete, spaced apart regions.

There Is No Reasonable Expectation that the Proposed Combination Would Be Successful

It is also respectfully submitted that there is no reasonable expectation that the combination of Fischer, Chen and Mitani would be successful.

In addition to the fact that, by combining Fischer, Chen and Mitani, a fuse fabrication method that lacks patterning of a "layer of conductive material to define at least two laterally discrete, spaced apart regions of conductive material between and around which [an underlying] insulative structure is exposed", it is respectfully submitted that one of ordinary skill in the art could not reasonably expect the combination of Fischer with Mitani to successfully result in the method recited in claim 18. Of particular note is the lack of disclosure of a multi-layered fuse having a metal silicide element as the portion of the fuse to be ruptured, or the use of spaced apart regions of polysilicon adjacent both the terminal portions of the metal silicide and an insulative structure of the semiconductor device. It is respectfully submitted that there is no reasonable expectation that the combination of these methods for forming a fuse render obvious a method for fabricating a fuse which includes the elements of claim 18. Rather, such a fuse would include a polysilicon element as the central portion of the fuse and spaced apart regions of metal silicide, aluminum, or tungsten.

Moreover, as the fuse fabrication method described in Mitani lacks patterning of a "layer of conductive material to define at least two laterally discrete, spaced apart regions of conductive material between and around which said insulative structure is exposed", it is respectfully submitted that any combination of Fischer, Chen, and Mitani would fail to result in the method recited in claim 18 and independent claim 17 from which claim 18 depends.

The Proposed Combination Does Not Teach or Suggest Each and Every Claim Element

Moreover, with respect to the fuse fabrication process described in Mitani, there is no teaching or suggestion of patterning a conductive layer, such as the polysilicon layer thereof, to form at least two laterally discrete, spaced apart regions between and around which regions of an underlying insulative structure are exposed. Further, there is no teaching or suggestion of a method of fabricating a fuse with a central portion formed of metal silicide spaced apart regions of polysilicon. As each of Fischer, Chen, and Mitani fails to teach or suggest these elements of claims 17 and 18, it is respectfully submitted that the Fischer, Chen, and Mitani cannot in combination teach or suggest these elements.

For these reasons, it is respectfully submitted that, under 35 U.S.C. § 103(a), claim 18 is allowable over the combination of Fischer, Chen, and Mitani and requested that the rejection of claim 18 under 35 U.S.C. § 103(a) be withdrawn.

Fischer, Chen, and Further in View of Sandhu

Claim 25 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Fischer and Chen as applied to claim 17 above, and further in view of U.S. Patent No. 5,231,056 to Sandhu (hereinafter "Sandhu").

The teachings of Fischer and Chen have been summarized above.

Sandhu teaches a process for depositing a tungsten silicide film on a substrate using chemical vapor deposition.

Claim 25 and independent claim 17 from which claim 25 depends recite chemical vapor depositing a layer of metal silicide over a semiconductor device, including adjacent to the regions of conductive material and the insulative structure exposed around the regions.

Claim 25 is allowable, among other reasons, as depending from claim 17, which should be allowed.

Fischer in View of Mitani and Chen

Claims 50, 51, 55-60, and 62-68 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Fischer in view of Mitani and Chen.

The teachings of each of these references have been summarized above.

One of Ordinary Skill in the Art Would Not Have Been Motivated to Make the Proposed Combination

For the same reasons provided above with respect to claim 18, it is respectfully submitted that one of ordinary skill in the art would not have been motivated to combine the teachings of Fischer, Mitani, and Chen in the manner that has been suggested in the outstanding Office Action.

There Is No Reasonable Expectation that the Proposed Combination Would Be Successful

In addition, for the same reasons provided above with respect to claim 18, it is respectfully submitted that there is no reasonable expectation that the combination of Fischer, Mitani, and Chen would be successful in rendering obvious the method for fabricating a fuse as recited in claims 50, 51, 55-60 and 62-68.

The Proposed Combination Does Not Teach or Suggest Each and Every Claim Element

Moreover, it is respectfully submitted that Fischer, Mitani, and Chen, taken either alone or in combination, do not teach or suggest each and every element of claims 50, 51, 55-60 and 62-68.

Independent claim 50 recites a method for fabricating a fuse that includes, among other things, fabricating laterally discrete, spaced apart regions comprising polysilicon on an insulative structure and fabricating a fuse comprising a metal silicide. When the laterally discrete, spaced apart regions are fabricated, and before the overlying fuse is formed, an insulative layer that underlies the spaced apart regions comprising polysilicon is exposed between and around the spaced apart regions. The fuse is fabricated in such a way as to include a central region located adjacent the insulative structure and between the spaced apart regions, as well as at least two terminal regions on opposite ends of the central region and adjacent the spaced apart regions that comprise polysilicon.

The teachings of Fischer are limited to forming a *window* centrally through a conductive layer, which could not result in *laterally discrete, spaced apart* regions of a first layer of conductive material. When the second conductive layer is formed, the insulative structure is no longer exposed through the window. According to Fischer, the first layer of conductive material is not patterned to form laterally discrete, spaced apart regions until after the second layer of conductive material has been formed and covers any portions of the insulative structure that were previously exposed through the window. Further, in the method of Fischer, the insulative structure that underlies the conductive structure is not exposed *around* the subsequently formed laterally discrete, spaced apart regions until after the second conductive layer has been formed thereover and patterned.

In addition, Fischer teaches that polysilicon may be used to form a top layer of the fuse described therein, including the fusible element that extends between terminals of the fuse. Fischer does not teach or suggest that spaced apart regions may be formed from polysilicon.

Further, Fisher does not teach fabricating laterally discrete, spaced apart regions, exposing insulative structure between and around each of said spaced apart regions.

Mitani teaches a second layer with spaced apart regions of metal silicide. Mitani neither teaches nor suggests spaced apart regions comprising polysilicon.

The fuse fabrication method disclosed in Chen does not include fabricating laterally discrete spaced apart regions of any conductive material, let alone polysilicon.

As none of Fischer, Mitani, or Chen teaches or suggests a fuse fabrication method which includes "*fabricating laterally discrete, spaced apart regions* comprising polysilicon on an insulative structure of a semiconductor device, said insulative structure being exposed between and around each of said spaced apart regions" (emphasis supplied), as is recited in independent claim 50 it is respectfully submitted that there is no way for the combination of these references to teach or suggest this element of independent claim 50.

For these reasons, it is respectfully submitted that, under 35 U.S.C. § 103(a), independent claim 50 is allowable over the combination Fischer, Mitani, and Chen.

Each of claims 51, 55-60, and 62-68 is allowable, among other reasons, as depending either directly or indirectly from claim 50, which is allowable.

Therefore, it is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 50, 51, 55-60, and 62-68 be withdrawn.

Fischer, Mitani, Chen, and Degelormo

Claims 52-54, 69, and 70 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Fischer, Mitani, and Chen, as applied to claims 50 and 51 above, and further in view of U.S. Patent 5,242,859 to Degelormo et al. (hereinafter "Degelormo").

The teachings of Fischer, Mitani, and Chen have been summarized previously herein.

Degelormo merely teaches a chemical vapor deposition method for forming layers of conductively doped polysilicon. Degelormo includes no teaching or suggestion that the CVD

process thereof may be used to fabricate any part of a fuse or structures associated directly with a fuse, let alone laterally discrete, spaced apart regions comprising polysilicon over an insulative structure around and between which an underlying insulative structure is exposed.

Thus, Degelormo includes no teaching or suggestion that would remedy the deficiencies of Fischer, Mitani, and Chen with respect to their inabilities to have provided one of ordinary skill in the art with motivation to make the asserted combination.

Nor do the teachings of Degelormo provide one of ordinary skill in the art with any additional reason to believe that the teachings of Fischer, Mitani, Chen, and Degelormo could be successfully combined to provide a method for fabricating a fuse. In particular, Degelormo does not include any teaching or suggestion of "fabricating laterally discrete, spaced apart regions comprising polysilicon on an insulative structure of a semiconductor device, said insulative structure being exposed between and around each of said spaced apart regions", an element of the fuse fabrication process recited in claim 50, from which claims 52-54, 69, and 70 depend, which is also missing from Fischer, Mitani, and Chen.

Accordingly, it is respectfully submitted that, under 35 U.S.C. § 103(a), claims 52-54, 69, and 70, each of which depends from claim 50, are allowable over the combination of Fischer, Mitani, Chen, and Degelormo.

Further, each of claims 52-54, 69, and 70 is allowable, among other reasons, as depending either directly or indirectly from claim 50, which is allowable.

Therefore, it is respectfully requested that the Office withdraw the rejection of claims 52-54, 69, and 70 under 35 U.S.C. § 103(a).

Fischer, Mitani, Chen, and Further in View of Sandhu

Claim 61 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Fischer, Mitani, and Chen as applied to claims 50 and 60 above, and further in view of Sandhu.

Claim 61 is allowable, among other reasons, as depending from claim 50 and 60, which should be allowed.

Mitani in view of Fischer and Chen

Claims 71, 74-86, 88-96, and 101 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Mitani in view of Fischer and Chen.

The teachings of each of these references have been summarized above.

Independent claim 71 recites a method of fabricating a gate and a fuse that includes patterning regions of a layer of polysilicon to form laterally discrete, spaced apart regions of polysilicon around and between which an underlying field oxide region is exposed.

It is respectfully submitted that there are several reasons a *prima facie* case of the obviousness of claims 71, 74-86, 88-96, and 101 has not been established.

One of Ordinary Skill in the Art Would Not Have Been Motivated to Make the Proposed Combination

First, for the same reasons provided above with respect to claim 18, it is respectfully submitted that one of ordinary skill in the art would not have been motivated to combine the teachings of Mitani, Fischer, and Chen in the manner that has been suggested in the outstanding Office Action.

There Is No Reasonable Expectation that the Proposed Combination Would Be Successful

Second, for the same reasons provided above with respect to claim 18, it is respectfully submitted that there is no reasonable expectation that the combination of Mitani, Fischer, and Chen would be successful in rendering obvious the method for fabricating a fuse as recited in claims 71, 74-86, 88-96, and 101.

The Proposed Combination Does Not Teach or Suggest Each and Every Claim Element

Finally, it is respectfully submitted that Mitani, Fischer, and Chen, taken either alone or in combination, do not teach or suggest each and every element of independent claim 71.

Specifically, none of Mitani, Fischer, or Chen teaches or suggests a fuse fabrication method that includes "patterning at least regions of [a] layer of polysilicon disposed over at least one field oxide region . . . to define at least two laterally discrete, spaced apart regions from said polysilicon over said at least one field oxide region with portions of said at least one field oxide region being exposed laterally around each of said spaced apart regions and therebetween" or "disposing a layer of metal silicide on said layer of polysilicon and into contact with said [exposed] portions of said at least one field oxide region".

Rather, in the fabrication method of Mitani, the first layer of polysilicon is not patterned until the metal silicide layer has also been deposited. See Fig B, C. The metal silicide layer does not contact the field oxide region, rather is deposited upon the polysilicon.

The teachings of Fischer are limited to forming a window centrally through a conductive layer, which could not result in *laterally discrete, spaced apart* regions of a first layer of conductive material around and between which an underlying insulative structure is exposed. According to Fischer, no laterally discrete, spaced apart regions of the first layer of conductive material are formed until after the second layer of conductive material has been formed.

Chen neither teaches nor suggests disposing multiple layers to fabricate a fuse, nor patterning said layers.

As none of Mitani, Chen, or Fischer teaches or suggests patterning at least regions of a layer of polysilicon in the manner recited in independent claim 71, any combination of these references also fails to teach or suggest this element of claim 71.

In view of the foregoing, it is respectfully submitted that, under 35 U.S.C. § 103(a), amended independent claim 71 is allowable over the combination of Fischer, Mitani, and Chen.

Claims 74-86, 88-96, and 101 are each allowable, among other reasons, as depending either directly or indirectly from claim 71, which should be allowed.

For the foregoing reasons, it is respectfully requested that the Office withdraw the 35 U.S.C. § 103(a) rejections of claims 71, 74-86, 88-92, and 101.

Mitani, Fischer and Chen, and Further in View of Degelormo

Claim 72 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Mitani, Fischer and Chen, as applied to claim 71 above, and further in view of Degelormo et al.

Claim 72 is allowable, among other reasons, as depending from claim 71, which should be allowed.

Mitani, Fischer and Chen, and Further in View of Sandhu

Claim 87 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Mitani, Fischer and Chen as applied to claim 71 above, and further in view of Sandhu.

Claim 87 is allowable, among other reasons, as depending from claim 71, which should be allowed.

Mitani, Fischer and Chen, and Further in View of Ukeda

Claims 97-100 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Mitani, Fischer and Chen as applied to claim 71 above, and further in view of U.S. Patent No. 6,069,055 to Ukeda et al. (hereinafter "Ukeda").

The teachings of each of Mitani, Chen, and Fischer have been summarized previously herein.

Ukeda teaches a dry etch process for anisotropically removing exposed regions of a polysilicon layer through a metal silicide layer. Ukeda does not teach or suggest that the process disclosed therein may be used in fabricating a fuse.

Accordingly, it is clear that Ukeda does not remedy the deficiencies of Mitani, Chen, and Fischer, and the knowledge that was generally available in the art prior to the filing date of the above-referenced application with respect to providing some motivation to one of ordinary skill in the art to combine the teachings of these references. It is also clear that Ukeda does not include any teaching that would give one of ordinary skill in the art a reasonable basis for expecting the combination of Mitani, Chen, Fischer, and Ukeda to provide a successful method for fabricating a fuse.

Claims 97-100 are each allowable, among other reasons, as depending from claim 71, which should be allowed.

Accordingly, it is respectfully requested that the 35 U.S.C. § 103(a) rejections of claims 97-100 be withdrawn.

CONCLUSION

It is respectfully submitted that each of claims 17-33, 50-72, and 74-101 is allowable. An early notice of the allowability of each of these claims is respectfully solicited, as is an indication that the above-referenced application has been passed for issuance. If any issues preventing the allowance of the above-referenced application remain which might be resolved by way of a telephone conference, the Office is kindly invited to contact the undersigned attorney.

Respectfully Submitted,

Brick G. Power
Registration Number 38,581
Attorney for Applicant
TRASKBRITT, PC
P.O. Box 2550
Salt Lake City, Utah 84110
Telephone: (801) 532-1922

Date: July 16, 2002

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